

HTCC substrate design rules

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1. Introduction

Process line situation introduction

The main technical specifications of the HTCC substrate are as follows:

- Standard thickness of each layer of ceramic: 0.15mm, 0.2mm, 0.25mm (cooked porcelain)
- The finest line and line spacing (thick film process): 100μm (cooked porcelain)
- Minimum hole spacing: 3 times aperture (universal)
- Metallized through hole diameter (raw porcelain): 200μm (universal, cooked ceramics about 170μm);
150μm (universal, cooked porcelain about 125μm);
100μm (minimum, mature porcelain about 85μm);
300 μm (maximum, mature porcelain about 250 μm).
- Maximum thickness of product: 5.0mm (cooked porcelain)
- Resistance of the wire: 15-18mΩ/□
- Metallized φ100μm through-hole column resistance: ≤30mΩ/mm;
Metallized φ150μm through-hole column resistance: ≤20mΩ/mm;
Metallized φ200μm through-hole column resistance: ≤15mΩ/mm;
Metallized φ300μm Through-hole column resistance: ≤10mΩ/mm.

Material system available

Alumina ceramics:

Al-Ca-Si-Mg (white porcelain, 94%-95%) AW01

Al-Ca-Si-Mg-Ti-Cr-Mo (black porcelain, 93%-94%) AB01

Al-Ca-Si-Mg-Cr-Mo (black porcelain, 93%-94%, requires split products)
AB01L

a. Acceptable design file format

Dwg, dxf, PROE, PROTEL format

b. Characteristic parameters

White porcelain:

● Dielectric constant:

$\epsilon_r = 9.1 \pm 0.2$ @DC-18GHz

$\epsilon_r = 9.3 \pm 0.2$ @18-40GHz

● Dielectric loss:

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$Tg\delta < 1.5 \times 10^{-3}$ @ DC-40GHz

● Insulation characteristics:

Breakdown voltage: $\geq 8000V/mm$

Insulation resistance: $\geq 10^{14} \Omega \cdot cm$ (20°C)

● Standard 50 Ω with line:

Insertion loss: $\leq 0.3dB/inch$ (X-band)

Standing wave ratio: < 1.2 (X band)

● Other material parameters:

Flexural strength: 350MPa

Yang Modulus: 304GPa

Thermal conductivity: 17W/m•K

Thermal expansion coefficient: 7-9ppm/°C (0-700°C)

Porosity: $\leq 4.5\%$ (SEM image method)

Black porcelain:

● Dielectric constant:

$\epsilon_r = 9.5 \pm 0.2$ @DC-18GHz

$\epsilon_r = 9.8 \pm 0.2$ @18-40GHz

● Dielectric loss:

$Tg\delta < 5.5 \times 10^{-3}$ @DC-40GHz

Flexural strength: 400MPa

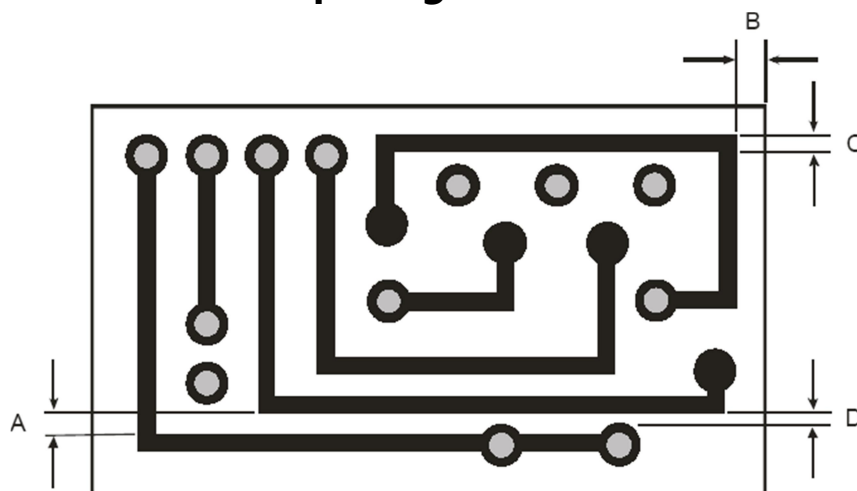
Yang Modulus: 304GPa

Thermal conductivity: 17W/m•K

Thermal expansion coefficient: 7-9ppm/°C (0-700°C)

Porosity: $\leq 4.5\%$ (SEM image method)

2. Line width and line spacing



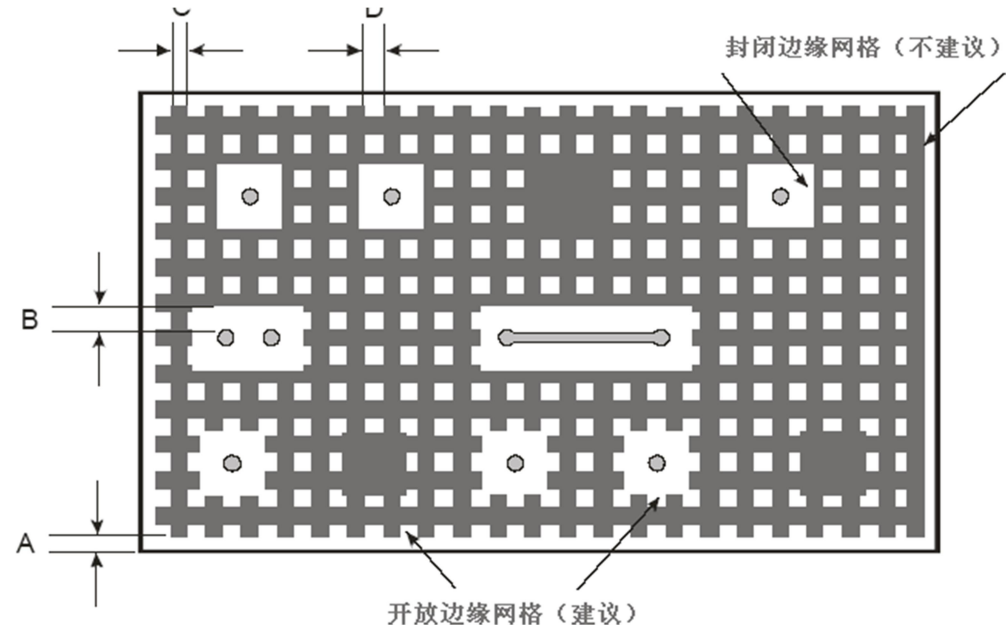
| | A | B | C | D |
|-------------|---------------------|----------------------|---------------------|----------------------|
| Recommended | $\geq 0.2\text{mm}$ | $\geq 0.15\text{mm}$ | $\geq 0.2\text{mm}$ | $\geq 0.20\text{mm}$ |
| Minimum | 0.10mm | 0mm | 0.10mm | 0.15mm |

1. It is recommended that the main conductor trace directions in each layer be as consistent as possible, and the main trace

directions of adjacent layers should be as perpendicular to each other as possible; The line radius/angle is too large to affect the minimum line spacing and its tolerance. It is recommended that the wiring be as vertical or parallel as possible, within the dense pattern. The blank space at the corner should be $\geq 0.25\text{mm}$.

- 2. The corners of the wire should be designed as rounded corners. The wires that are not connected to the holes should be terminated by circular pads.
- 3. In the above values, A and D must satisfy the conditions at the same time;

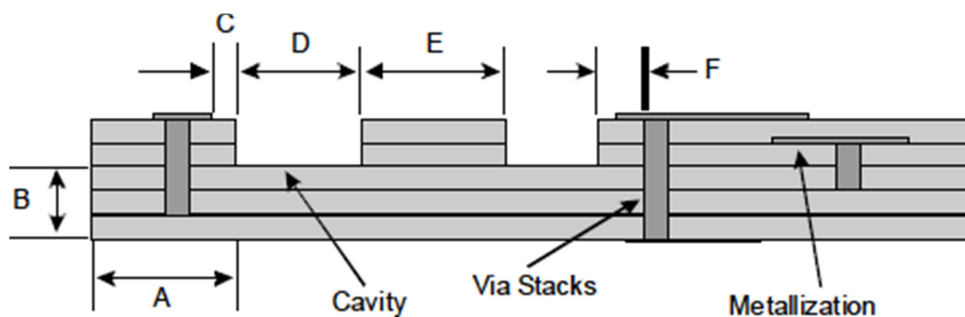
3. Ground plane / power plane



| | A | B | C | D |
|--------------|---------------------|---------------------|---------------------|---------------------|
| Recomm ended | $\geq 0.2\text{mm}$ | $\geq 0.2\text{mm}$ | $\geq 0.4\text{mm}$ | $\geq 0.4\text{mm}$ |
| Minimu m | 0 | 0.15mm | 0.1mm | 0.1mm |

1. The ground plane/power plane of the middle layer should be gridded as much as possible;
2. The similar ground plane / power plane should have a certain offset, or use a different grid pattern;
3. The grounding surface/power surface metallization pattern should be evenly distributed on the ceramic strip, and the metal pattern area should not exceed 75%.

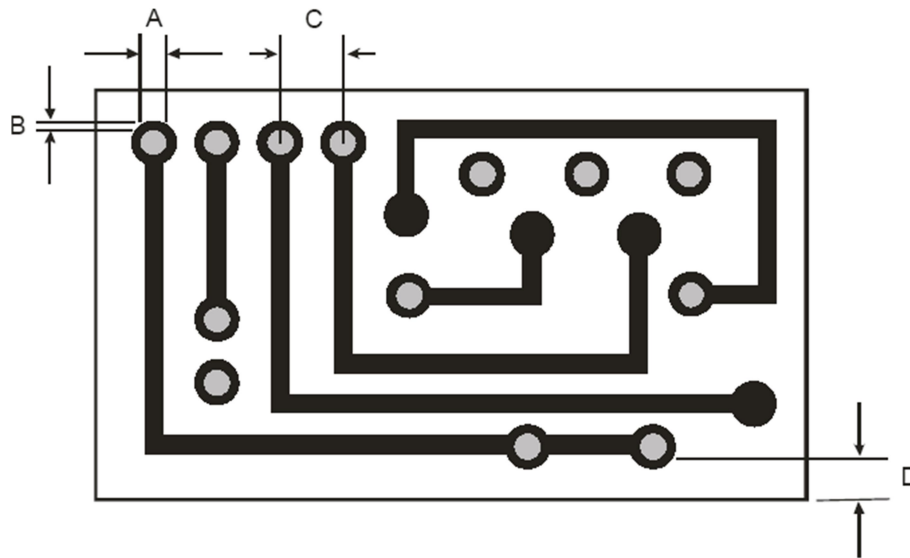
4. Cavity



| | A | B | C | D | E | F |
|-------------|---------------------|---------------------|----------------------|---------------------|---------------------|---------------------|
| Recommended | $\geq 0.8\text{mm}$ | $\geq 0.4\text{mm}$ | $\geq 0.15\text{mm}$ | $\geq 1.0\text{mm}$ | $\geq 0.8\text{mm}$ | $\geq 0.5\text{mm}$ |
| Minimum | 0.5mm | 0.2mm | 0 | 0.5mm | 0.5mm | 0.25mm |

1. The cavity should be rectangular or circular as much as possible, and other irregular structures should be processed;
2. If there is a metallized pattern inside the cavity, the depth of the cavity should not be more than 2 times the width.

5. Through hole



| | A | B | C | D |
|-------------|--------|---------------------|-------------------------------|---------------------|
| Recommended | 0.2mm | $\geq 0.1\text{mm}$ | $\geq 3 \times \text{than A}$ | $\geq 0.5\text{mm}$ |
| Minimum | 0.10mm | 0.05mm | $2.5 \times \text{than A}$ | 0.3mm |

1. hole is generally round, commonly used standard aperture 0.15mm, 0.20mm, 0.30 mm;
2. Control the number of holes as much as possible while maintaining electrical performance.
3. It is not recommended to use through-holes. It is recommended that the through-holes in the same position, more than 3 layers, be staggered every 3 layers, offset. It is recommended to be larger than 1.5 times the aperture to avoid the accumulation of the filling holes;

6. Multilayer ceramic package design rules

Fired shape

| | | | |
|-----------------|------------------------------|-------------------------|---------------------|
| Item | | Standard | Special |
| Size | | ≤100SQ | ≤150SQ |
| Layer thickness | | 0.15—0.3mm Total≤4mm | 0.10mm Total≤5mm |
| ΔR | Dimension | ±0.8% ≤±0.03 mm | ±0.5% ≤±0.02 mm |
| | Dimension in different layer | ±0.8% ≤±0.10 mm | ±0.5% ≤±0.05 mm |
| | Thickness | ±10% | ±3% ≤±0.02 mm |
| | Cavity size | ±1.0% | ±0.8% |
| Warpage | | 3um/mm | 1um/mm |